WHAT IS CLAIMED IS:

1	1. A method for processing integrated circuit devices, the method		
2	comprising:		
3	providing a monitor wafer, the monitor wafer comprising a silicon material;		
4	introducing a plurality of particles within a depth of the silicon material,		
5	whereupon the plurality of particles cause the silicon material to be in an amorphous state;		
6	introducing a plurality of dopant particles into a selected depth of the silicon		
7	material using an implantation tool, the amorphous state trapping the dopant particles;		
8	subjecting the monitor wafer including the plurality of particles and dopant		
9	particles into thermal anneal process to activate the dopant;		
10	removing the monitor wafer;		
11	measuring a sheet resistivity of a surface region including the implanted		
12	dopant particles of the monitor wafer;		
13	determining a dose of the dopant bearing impurities; and		
14	operating the implantation tool using one or more production wafers if the		
15	dose of the dopant particles in the monitor water is within a tolerance of a specification limit.		
1	2. The method of claim 1 wherein the monitor wafer is substantially fre		
2	of screen oxide overlying a surface of the monitor wafer.		
1	3. The method of claim 1 wherein the plurality of particles are silicon		
2	bearing impurities.		
2	bearing impurities.		
1	4. The method of claim 3 wherein the silicon bearing impurities are		
2	implanted using a dose of 1 X 10 ¹⁵ atoms/cm ² and an energy of 20 keV.		
1			
1	5. The method of claim 1 wherein the dopant particles are boron bearing		
2	impurities.		
1	6. The method of claim 5 wherein the boron bearing impurities are		
2	implanted using a dose ranging from about 5 X10 ¹³ through 4 X 10 ¹⁴ atoms/cm ² and an		
3	energy ranging from about 1-2 keV.		
1			
1	7. The method of claim 1 wherein the thermal anneal process is an RTP		
2	process at about 700 Degrees Celsius.		

1	8. The method of claim 1 wherein the thermal anneal process is an RTF	.	
2	process ranging from about 650 to 750 Degrees Celsius.		
1	9. The method of claim 1 wherein the thermal anneal process is a rapid		
2	thermal anneal process.		
_	thermal annoar process.		
1	10. The method of claim 1 wherein the sheet resistivity is provided in a		
2	separate tool.		
1	11. The method of claim 1 wherein the operating of the production wafe	ers	
2	occurs for 24 hours after determining the dose of the dopant impurities.		
	and the same second sec		
1	12. The method of claim 1 wherein the thermal anneal process also		
2	recrystallizes a portion of the amorphous silicon.		
1	13. A method for processing semiconductor waters, the method		
2	comprising:		
3	providing a monitor wafer, the monitor wafer comprising a crystalline		
4	material;		
5	introducing a plurality of particles within a depth of the material, whereupon	n	
6	the plurality of particles cause the crystalline material to be in an amorphous state;		
7	introducing a plurality of dopant particles into a selected depth of the		
8	crystalline material in the amorphous state using an implantation tool, the amorphous state		
9	trapping the dopant particles;		
10	subjecting the monitor wafer including the plurality of particles and dopant		
11	particles into thermal anneal process to activate the dopant;		
12	removing the monitor wafer;		
13	measuring a sheet resistivity of a surface region including the implanted		
14	dopant particles of the monitor wafer;		
15	determining a dose of the dopant bearing impurities; and		
16	operating the implantation tool using one or more production wafers if the		
17	dose of the dopant particles in the monitor water is within a tolerance of a specification limit.		
1	12 The mosthed of claims 10 and and a set 11' and a set 11'		
1	13. The method of claim 12 wherein the crystalline material comprises		
2	silicon.		

1	14.	The method of claim 12 wherein the dose of the dopant bearing	
2	impurities is determined using a relationship between resistivity values and dose values.		
1	15.	The method of claim 14 wherein the relationship has been provided in	
2	a spatial plot.		
1	16.	The method of claim 12 wherein the plurality of particles comprise	
2	silicon bearing particles.		
1	17.	The method of claim 12 wherein the dopant bearing impurities	
2	comprise boron species.		
1	18.	The method of claim 11 wherein the monitor water is substantially free	
2	from an overlying oxide layer before introducing the dopant bearing impurities.		
1	19.	The method of claim 11 wherein the monitor wafer is silicon wafer.	
1	20.	The method of claim 11 wherein the one or more production wafers is	
2	characterized by a shallow junction depth of less than about 40 nm.		